A 5–6-GHz Bipolar Quadrature-Phase Generator

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***Abstract*—A wide-band fully monolithic quadrature-phase generator is implemented. It consists of a bipolar frequency doubler with differential outputs and a regenerative divider with 5 mV_{rms} maximum sensitivity. Measured residual phase noise is $< \pm 0.5$ dB for offsets between 100 Hz and 100 kHz in the 5–6-GHz band, limited by the resolution of the measurement equipment. An electronic phase tuning circuit controls the I/Q phase error to $\pm 15°$ of tuning range with 0.033°/mV sensitivity. Unwanted harmonics are suppressed by over 40 dB within the working range of the multiplier. The test circuit occupies an active area of 0.26×0.11 mm^2, and consumes 23 mW from a 2.7-V supply.**

***Index Terms*—Frequency division, frequency multiplication, phase noise, quadrature phase generator, regenerative quadrature divider, wireless local-area networking.**

I. Introduction

WIRELESS local area networks (WLANs) are projected to steadily increase in number and in the data traffic they handle over the coming decade. With products already operating in the congested 2.4-GHz ISM band, broadband WLAN development is now also aimed at operation in the 5–6-GHz band. In addition to higher data rates, the cumulatively larger available spectrum—300 MHz for IEEE 802.11a in the 5–6-GHz band versus 83.5 MHz for 802.11b at 2.4 GHz—makes migration to the 5-GHz band appealing. As system operating frequencies move into higher frequency bands, the design of quadrature oscillators as sources of high-frequency signals with adequate output power becomes increasingly difficult, costly, and inconvenient.

Single-sideband transceiver architectures (both homodyne and heterodyne) are widely used in RF integrated circuits to relax off-chip filtering requirements. A quadrature-phased local oscillator (LO) is needed, where the in-phase (I) and quadrature (Q) signals are typically sourced by either a multistage (i.e., quadrature) voltage-controlled oscillator (VCO) [1] or an oscillator followed by a passive polyphase filter [2]. Phase and amplitude precision between the I and Q outputs depends upon circuit topology and processing variations, and electronic trimming of the I-Q phase difference is difficult to implement. A two-stage *RC* polyphase filter designed for the 5–6-GHz band requires approximately 0.18×0.18 mm^2 of chip area, has an insertion loss of 3 dB, and sideband rejection is between 35 and 40 dB (limited by phase and amplitude errors in a transceiver). This can be improved by increasing the number of filter stages, but comes at the cost of increased chip area and insertion loss.

An I-Q VCO requires double the chip area and can more than double the power consumption of a single-stage oscillator/buffer. More importantly, however, the power consumption of quadrature oscillators cannot be optimized independent of phase noise considerations [3]. In a properly designed differential Colpitts oscillator, an impulse of current is delivered to the tank when the voltage across the tank is close to its peak value, which helps to minimize phase noise as described in [3]. In a quadrature VCO there are two tanks which must be excited 1/4 cycle apart in time. The minimum amount of energy required to sustain an oscillation in a circuit with two independent resonators excited by an impulse of current is therefore double that of a single-stage VCO. In practical circuits, it has been shown that coupled VCOs operate slightly off-resonance [1], and therefore additional power is consumed to realize a desired level of phase noise compared to a single-stage oscillator (assuming identical resonators). This deficiency can be corrected through circuit modifications. However, alterations such as coupling the I and Q stages via cascode devices as in [1] requires additional supply headroom which also increases power consumption. For example, the 1.8-GHz I-Q VCO described in [1] is implemented in 0.35-μm CMOS and demonstrated -140 dBc phase noise at 3-MHz offset, while consuming 25 mA from a 2-V supply. The same author reported a 1.8-GHz single-stage VCO designed in the same technology [4] that has similar phase noise performance (-138.5 dBc/Hz at 3-MHz offset), but consumes just 6 mA from a 2-V supply—less than one-quarter the power consumption of the I-Q VCO. We note that to realize the same phase noise would require an increase in bias current for the single-stage oscillator. However, as a 3-dB improvement in the phase noise theoretically requires double the power consumption, our assertion that an I-Q VCO requires double the power consumption of a single-stage equivalent is confirmed by these results from the literature.

A wide-band frequency multiplier and regenerative divider in cascade (see Fig. 1) is potentially a low-power, small chip area solution for generating quadrature signals in a wireless transceiver. Additionally, the multiplier and divider cascade allows a single VCO to be shared between the transmit and receive circuits on-chip. Passive multipliers consume little dc power, but typically have a low output voltage swing due to conversion losses in multiplication. The input sensitivity of a regenerative divider near its self-oscillating frequency is on the order of a few millivolts, making it compatible with a passive multiplier. The potential for low-power operation was proven in [5], where a SiGe bipolar regenerative multiplier with quadrature

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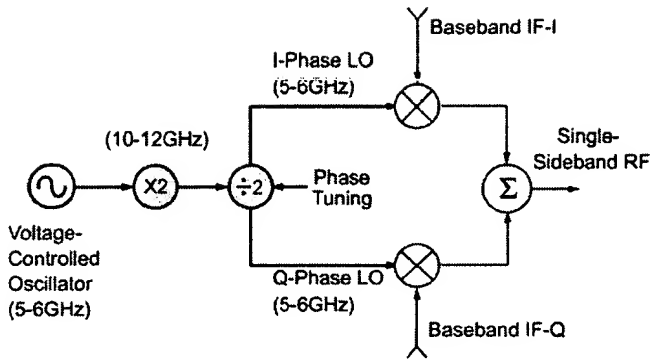

Fig. 1. Quadrature phase generation in an upconverter.

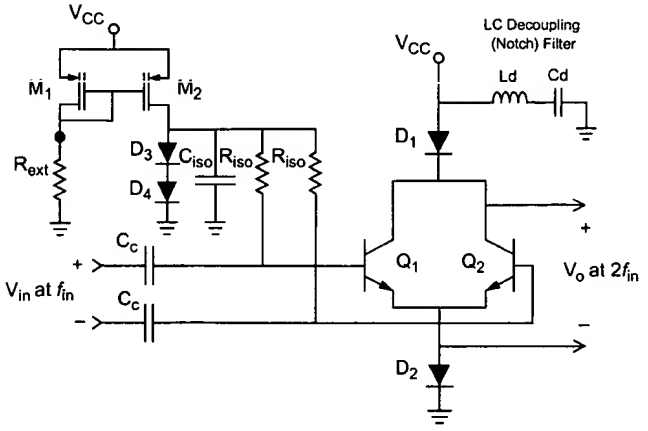

Fig. 2. Schematic of the differential frequency doubler with diode loads.

outputs demonstrated operation from 2.4–5.5 GHz while consuming just 220 μA from a 2-V supply. Overall, the current consumed by a multiplier/divider is potentially less than the current required by a two-stage (I/Q) VCO with dual output buffers. This is because in bipolar the divider consumes about the same amount of current as the oscillator buffers it replaces and its emitter follower outputs are capable of driving a mixer directly, while the multiplier could consume less than an additional oscillator stage. In addition, phase noise and current consumption of each block in the LO chain (i.e., VCO, multiplier, and divider) can be optimized separately, and existing VCO designs can be leveraged to reduce time to market and design cost.

A 2.7-V quadrature-phase generator for 5–6-GHz WLAN applications, based on a passive multiplier followed by a regenerative frequency divider is described in this paper [6]. The test circuits (shown as the shaded blocks in Fig. 1) are designed and fabricated in a 0.18-μm SiGe BiCMOS technology. The first-stage multiplier is based on a new circuit topology that has wide operating bandwidth and 0.5-mW standby power consumption. The measured residual phase noise of the multiplier, divider and multiplier/divider in combination, are characterized and found to be within the error limitations of the measurement equipment. The entire I/Q generator requires less chip area than a typical 5–6-GHz two-stage polyphase filter. Electronic tuning of the I and Q output phases is also implemented to maximize sideband rejection despite processing and temperature variations.

II. Frequency Multiplier

Frequency multipliers and dividers provide system design flexibility on an RF IC by eliminating the need to redesign an existing local oscillator. For example, an oscillator designed for a portable handset at 900 MHz could be reused in a 1800-MHz design by doubling the original frequency ($\times 2$ from 900 to 1800 MHz). For handheld devices, power consumption, spurious outputs, and chip area used to implement the circuit must also be considered.

A. Monolithic Multipliers

Traditional methods of microwave frequency doubling apply energy to a nonlinear passive device such as a varactor or step recovery diode in order to generate harmonics that are then filtered to select the desired frequency. However, this approach usually results in conversion loss when the input and output power levels are compared [7].

As operating bandwidth improves with technology scaling, transistor multipliers become attractive for frequency doubling and tripling in the low-gigahertz range because they can produce gain at the desired output harmonic. Despite this advantage, few of the existing transistor-based multiplier designs are compatible with monolithic integration and perform well at RF. Most monolithic multipliers exploit even-order nonlinearities to generate a double-frequency output and are based on single-ended rather than balanced circuit topologies [8]–[12]. Balanced circuits are preferred for the superior noise rejection and circuit-to-circuit isolation they offer in monolithic applications.

B. Fully Differential Wide-Band Multiplier

The wide-band frequency multiplier shown in Fig. 2 was developed to generate a 10–12-GHz differential signal (as in Fig. 1) on-chip. The 5–6-GHz I/Q signals are obtained subsequently by frequency division. Regenerative divide-by-2 circuits [11] consume less power and operate to higher input frequencies than digital dividers, but do not operate down to dc (i.e., they are narrow-band). Therefore, any constraint on the operating frequency from the multiplier stage further restricts the overall design margin given temperature and manufacturing variations. By using a wide-band multiplier circuit in the first stage, it is only the narrow-band divider in the second stage that determines the overall operating frequency range.

Balanced circuits, such as the differential pair, are preferred for their superior common-mode rejection in monolithic applications. Differential pair Q_1, Q_2 in Fig. 2 generates mainly even-order harmonics. Shorting the collectors ensures that the fundamental and odd-order harmonics are suppressed in the collector and emitter currents of the transistors when driven differentially. Since the collector and emitter currents are approximately equal, the voltages developed across matched diodes D_1 and D_2 are (ideally) also identical but opposite in phase (i.e., 180° phase-shifted). It should be noted that MOSFETs could be substituted for bipolar transistors in this topology without affecting overall circuit functionality.

The output amplitude can be predicted by considering the nonlinear response of the transistor. For a sinusoidal (differential-mode) input voltage V_{in} consisting of dc and ac components (i.e., $V_{\text{in}}/2 = V_{BE} + V_{\text{in}}\cos(\omega t)$) across the base-emitter of either Q_1 or Q_2 in Fig. 2, the collector current is

$$I_C = I_S e^{V_{\text{in}}/2V_T} = I_S e^{(V_{BE}+V_m\cos(\omega t))/V_T} = I_{dc}e^{k\cos(\omega t)}. \tag{1}$$

Here, I_{dc} is the dc bias current and k is the ratio of peak input to the transistor thermal voltage, $k = V_m/V_T$.

Expansion of the exponential $e^{k\cos(\omega t)}$ gives the collector current

$$I_C = I_{dc}I_0(k)\left[1 + \sum \frac{2I_n(k)}{I_0(k)}\cos(n\omega t)\right] \quad \text{for } n = 1, 2, 3, \ldots \tag{2}$$

where $I_n(k)$ are modified Bessel functions of the first kind [13].

The output at each harmonic is proportional to the dc bias current and input amplitude (V_m), since the ac differential output voltage V_o, is

$$V_o = 4I_{ac} \times r_{\text{load}}. \tag{3}$$

The resistance of the diode loads is r_{load} and I_{ac} is the time-varying part of (2).

In Fig. 2, the dc currents of both Q_1 and Q_2 flow through each diode load. Note that the diode resistance can be approximated by its small-signal resistance (r_{ac}) because the output voltage is typically on the order of a few tens of millivolts. The total load resistance is the sum of r_{ac} and the extrinsic resistance of the diode R_s

$$r_{\text{load}} = r_{ac} + R_s = \frac{1}{gm} + R_s = \frac{V_T}{(2 \cdot I_{dc}I_0(k))} + R_s. \tag{4}$$

From the product of the signal current and load resistance (ignoring other parasitics), the peak voltage across either diode is approximately

$$\begin{aligned} V_o &= 4I_{ac} \cdot r_{\text{load}} \\ &= 4\left(I_{dc}I_0(k)\sum \frac{2I_n(k)}{I_0(k)}\cos(n\omega t)\right) \\ &\quad \cdot \left(\frac{V_T}{2(I_{dc}I_0(k))} + R_s\right). \end{aligned} \tag{5}$$

For the second harmonic, $n = 2$ and (5) becomes

$$V_{o,n=2} \approx \frac{4V_T I_2(k)}{I_0(k)}\cos(2\omega t). \tag{6}$$

Note that the extrinsic resistance of the diode load is ignored and that the differential output is double the voltage drop across a single diode load.

For an input amplitude of $V_m = 0.5V_{pk}$ at room temperature, (6) predicts a peak differential output voltage of about 90 mV. Again, the actual output is somewhat larger due to the presence of the extrinsic resistances in the diode loads. The temperature dependence of $I_0(k)$ and $I_2(k)$ (where k and $I_n(k)$ decrease with increasing temperature) tends to compensate for the temperature dependence of V_T, which increases with increasing temperature.

Diode loads allow operation from a 2.7-V supply and provide a wide operating bandwidth as the ac resistance is typically on the order of tens of ohms. Computer simulations predict that the complete multiplier test circuit correctly doubles the input frequency up to 36-GHz output. To increase the output swing, small series resistors can be placed in series with the diodes (i.e., increase R_s). A bias current can also be used to increase the output amplitude, however, this comes at a cost of added power consumption. Finally, low voltage operation is realized by replacing the diode loads with resistor loads. This enables compatibility with deep-submicron IC technologies that operate from supplies at or below 1 V (e.g., 90-nm CMOS technologies), but will make the doubler output temperature dependent.

If resistors are substituted for the diode loads, the minimum supply voltage is the dc voltage drop across the resistors plus the transistor saturation voltage V_{CEsat}. For 200-Ω resistor loads with a dc bias of 250 μA and V_{CEsat} of 0.3 V (typical value), the minimum supply voltage is approximately 0.4 V. With diode loads, the minimum supply voltage is V_{CEsat} plus twice the diode forward voltage drop, which is 0.85–0.9 V for the BiCMOS process used here for fabrication. Thus, the minimum supply voltage using diode loads is about 2.1 V. The maximum supply voltage for a resistively loaded multiplier is determined by the breakdown of Q_1 or Q_2, which in practice lies between the collector-emitter (~2 V) and collector base (~6 V) breakdown voltages. Considering noise, the main source of noise in a resistor load is thermal, which is double the shot noise power of a diode load implementation for the same small-signal resistance, so the thermal noise floor would increase. Flicker noise is of minimal concern as the output frequency of the doubler circuit is high. Matching of the resistor loads is important as this affects the doubler's output amplitude matching. The temperature dependence is determined by the temperature dependence of $I_0(k)$ and $I_2(k)$ and the characteristics of the resistors, which could be made complementary depending on the resistor doping (e.g., n- or p-type polysilicon loads).

The maximum supply voltage with resistor loads is limited by breakdown voltage V_{CE0} (1.5–2 V). Therefore, the supply voltage range for a bipolar implementation is $2V_{BE} + V_{\text{CE0}} \approx$ 3.3 V. If 0.18-μm MOS devices were substituted for the transistors in the doubler circuit, the supply voltage range is approximately the same, assuming a V_{eff} of 0.3 V for the MOSFETs (which replace Q_1, Q_2 in Fig. 2).

The doubler core in the IBM SiGe-7HP technology has a simulated −3 dB output bandwidth of 78 GHz (i.e., from 3–81 GHz). The upper limit is restricted by the device parasitics, while the lower limit is set by ac coupling capacitors used at the multiplier inputs. Although the multiplier core can still generate doubled frequency outputs for inputs as low as 20 MHz and as high as 100 GHz, the output amplitude at these frequencies is on the order of 15 mV_{peak}.

The biasing circuit for the bases of transistors Q_1 and Q_2 is also shown in Fig. 2. Transistors M_1 and M_2 form a current mirror which is adjusted externally using R_{ext} to set the desired bias current for the test circuit. Diodes D_3 and D_4, which are

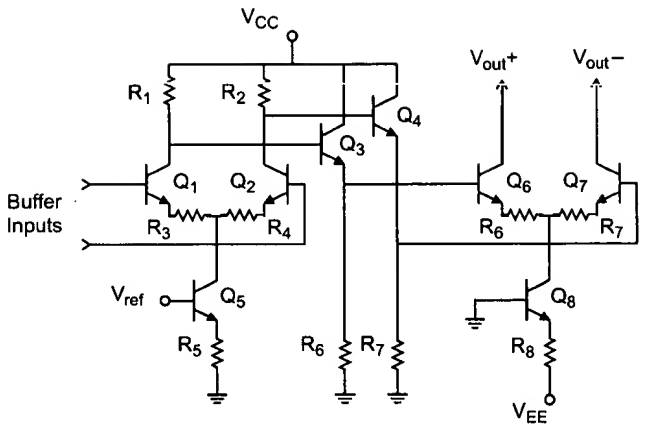

Fig. 3. Open-collector output buffer.

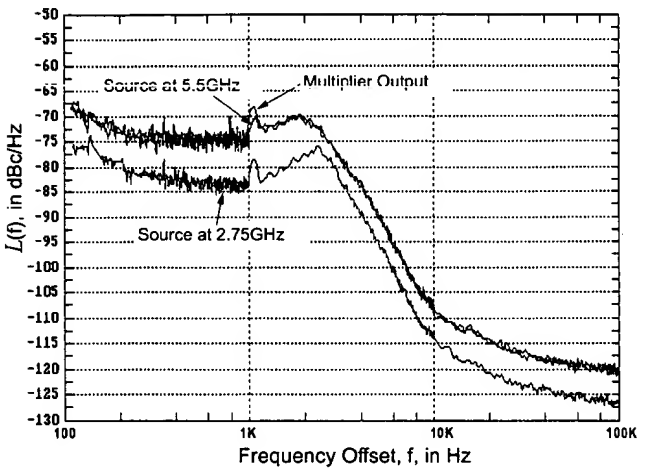

Fig. 4. Measured phase noise of source at 2.75 and 5.5 GHz compared to multiplier output for 2.75-GHz input.

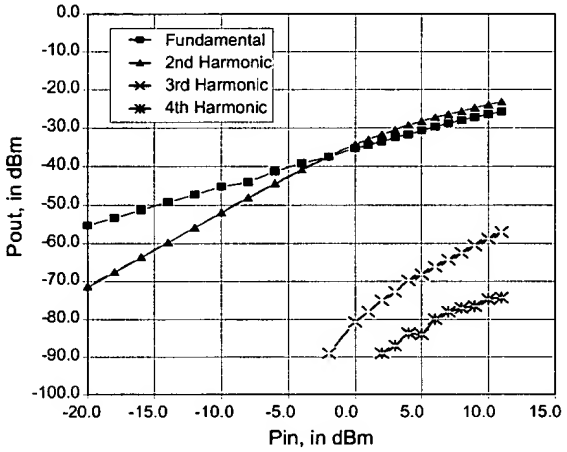

Fig. 5. Differential output power versus input power in dBm for the standalone multiplier test circuit for $f_{in} = 6.0$ GHz.

matched in area to Q_1 and Q_2, set a temperature tracking bias at the bases of the doubler transistors. There is a slight error in the bias current due to the finite current gain of the BJTs, but this on the order of 1%–2% as transistor dc beta is typically 100. A MOSFET equivalent would not have this bias current error. Resistors R_{iso} and decoupling capacitance C_{iso} provide isolation between the bias circuit and the RF input signals.

A standalone test circuit for the multiplier was designed and fabricated. Input and output buffer circuits were added to facilitate testing. Emitter-followers with 50-Ω termination resistors across their RF inputs buffer signals into the multiplier core. The open-collector output buffer (shown in Fig. 3) consists of differential pair buffer (Q_1, Q_2) followed by an open-collector output pair (Q_6, Q_7). The 50-Ω impedance of the test gear serves as the load. Output swing of the open collector stage is set by the product of the 50-Ω load impedance and bias current: $V_{swing} = 50\ \Omega \times I_{bias}$. To realize a 0.5-$V_{peak}$ output swing (per output, single-ended), a bias current of approximately 10 mA is used.

Measurements of the multiplier's phase noise output at 5.5 GHz are plotted in Fig. 4 along with the noise of the input source at 2.75 and 5.5 GHz. The measurement is made at 5.5 GHz due to the 6-GHz limit of the measurement system. The expected theoretical difference of 6 dB (i.e., 20log(5.5/2.75)) is seen between the source at 2.75 GHz and its doubled output at 5.5 GHz over the entire range. The discrepancy seen between the doubled source output (at 5.5 GHz) and the source itself when set to 5.5 GHz (i.e., not doubled) is also on the order of the measurement error. The multiplier core consumes 12.5 mW from a 2.7-V supply when driven by a 0.5-V_{peak} differential input, and the packaged test circuit has a conversion loss of 18.7 dB from input to doubled output. Part of the conversion loss is caused by bondwire and lead self-inductances (~3 nH) which attenuate the input and output. Fig. 5 displays the strong harmonic suppression of the multiplier at 6-GHz input. Note that the conversion from fundamental to the second harmonic is linear for low input powers but saturates as the input power increases above approximately 0 dBm. The fundamental component results from poor isolation between the input and output due to the 32-pin ceramic quad flatpack (CQFP) used for testing, which has lower isolation than the test circuit itself.

III. Multiplier Supply Decoupling

Proper supply decoupling is important for the multiplier as there is little attenuation between the supply pins and the output. Without adequate decoupling, the double frequency component can couple via either power or ground supplies to other circuit blocks. Also, stray signals entering the core circuit may corrupt the balanced differential output.

Despite the desire for large capacitance values in decoupling applications, the physical size of an integrated capacitor is limited by the available chip area. For example, decoupling the 10–12-GHz doubled signal with a reactance of 1 Ω at 10 GHz requires a 16-pF on-chip capacitor and 32 000 μm^2 of chip area at a density of 0.5 $fF/\mu m^2$.

As an alternative, the series LC filter shown in Fig. 6 was developed. The notch filter's reactance drops to zero at the resonant frequency $\omega_0 = 1/\sqrt{LC}$, with a bandwidth determined by the Q of the capacitor and inductor. As bandwidth is inversely proportional to the Q of the circuit, there is a tradeoff between designing the notch filter to have a bandwidth wide enough to cover its necessary operating range and the filter's Q factor.

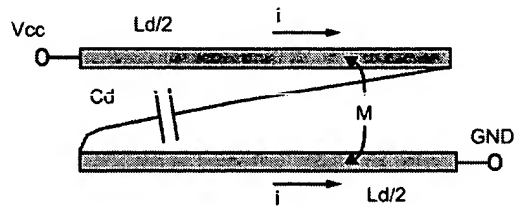

Fig. 6. *LC* supply decoupling filter.

For a 10–12-GHz application, the inductance value required when using a 0.5-pF capacitor is

$$L = \frac{1}{(2\pi f_0)^2 C} = \frac{1}{(2\pi(11\text{ GHz}))^2 0.5\text{ pF}} \approx 0.4\text{ nH}. \quad (7)$$

For space saving purposes, the inductance is implemented using two microstrip lines as shown in Fig. 6. Mutual coupling M between the metal lines increases the net inductance as ac current (i) flows in the same direction in both lines. The series resistance of the filter at resonance is 1.2 Ω. The total area occupied by the *LC* decoupling filter implemented for the multiplier is 12 880 μm^2, or a 60% saving of space compared to simple capacitive decoupling. Manufacturing defects caused by pinholes in the insulator of a high-density on-chip (e.g., MIM) capacitor are less likely when a smaller area is used, thereby improving the circuit yield. The chip area required for the capacitor in this case is reduced by a factor of 30 (0.5 pF versus 16 pF).

IV. Frequency Divider

Both digital dividers using sequential logic and analog circuits based on multiplication-with-feedback loops are commonly used for frequency division. A digital divide-by-two requires a single D-type flip-flop with the inverting ($\overline{Q}$) output fed back to the D input. The flip-flop is typically implemented in a master/slave topology using current steering logic (such as emitter-coupled bipolar or source-coupled FET logic), and operation from dc to one-half of the transistor transit frequency (f_T) can be realized [14], [15]. High-speed latches are required for master and slave, with each latch consisting of an input buffer and regenerative stage biased by a common current source. I and Q signals are available at the master and slave outputs when the circuit is driven by a 50% duty cycle clock. For operation in the gigahertz range, active devices in these circuits are biased close to peak f_T, however, this consumes a relatively large supply current.

Analog dividers typically consumes less power than a digital divider and operates right up to the transistor f_T, or about double the maximum operating frequency of a digital divider implemented in the same technology [16], [20]. This is advantageous in portable RF front-ends where battery power must be conserved in circuits that are narrow-band in that they do not require operation down to dc. A divider using the multiplier-with-feedback scheme proposed by Miller and Fortescue is shown in Fig. 7(a) [17], [18]. In continuous operation, input frequency $2f_{LO}$ is multiplied by f_{LO} to give sum and difference components at $3f_{LO}$ and f_{LO} at the multiplier output. Lowpass

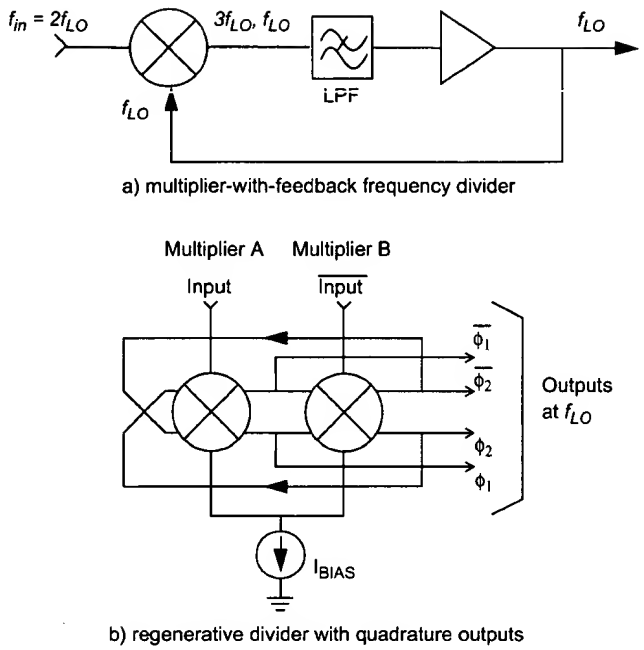

Fig. 7. Regenerative frequency division.

filtering removes the component at $3f_{LO}$, and gain in the multiplier and buffer amplifier ensure sufficient loop gain for sustained operation. The scheme is regenerative because the overall loop gain is greater than one at the desired output frequency, f_{LO}. In general, both integer and fractional divide-by-N circuits are possible using this scheme if additional multipliers are added in the feedback and input paths [19].

A. Regenerative Frequency Divider With Quadrature Outputs

An extension of the multiplier-with-feedback concept that implements a divide-by-2 with quadrature outputs is shown in Fig. 7(b) [5]. Two active multipliers with balanced inputs are cascaded in a positive feedback loop so that each multiplier contributes exactly 90° phase shift to the divided output signal, independent of the input frequency. The input signal at $2f_{LO}$ is fed in-phase and anti-phase into multipliers A and B, respectively. Conversion gain from the multipliers provides the loop gain needed for regeneration of the f_{LO} output. Each multiplier has a low-pass response that removes the unwanted component at $3f_{LO}$. Outputs ϕ_1 and ϕ_2 are in precise phase quadrature (i.e., within 1° phase error, or less) with equal output amplitudes when the components in each stage are matched.

At very low frequencies, the phase shift across each multiplier stage is less than 90° and so regeneration cannot be sustained. Also, at very high frequencies, the conversion gain of each multiplier is insufficient to sustain regeneration and there will be no stable output. When synchronized, the divider is injection-locked to the input at $2f_{LO}$ with output f_{LO}. Therefore, the output signal tracks the $2f_{LO}$ input signal both in frequency and phase. In addition, the phase noise at the output tracks the phase noise of the $2f_{LO}$ input signal. The input phase noise spectral density is (theoretically) 6 dB larger than the output as a result of frequency division by two.

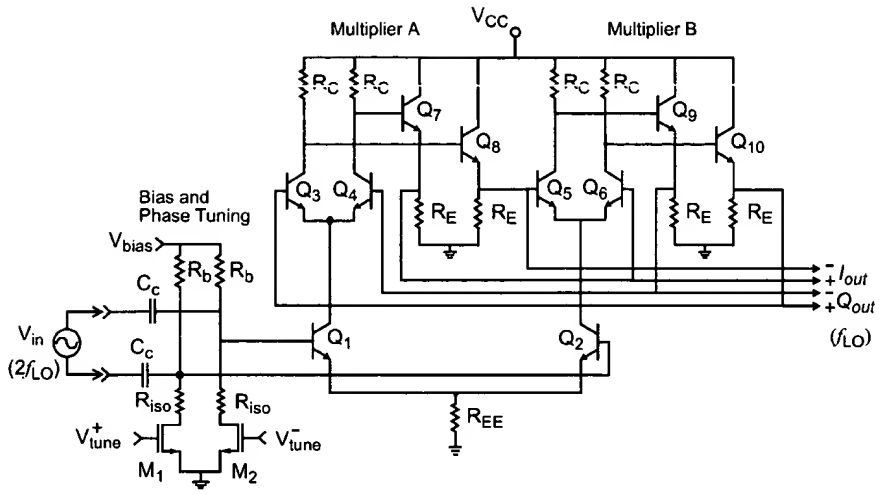

Fig. 8. Quadrature regenerative divider.

A schematic of the quadrature divider test circuit is shown in Fig. 8. While sharing topological similarities with master/slave digital dividers, this regenerative analog circuit uses fewer transistors and can be implemented using either MOS or bipolar transistors. A mainly bipolar circuit is used here. Collector loads (R_C), parasitic capacitance at the collector node, and the emitter follower buffers low-pass filter the output to ensure that the divide-by-2 frequency component dominates in the feedback loop. Emitter-follower buffers (Q_7–Q_{10}) also provide level shifting and buffering between the multiplying stages. Bias current in shared by the two transistors in the lower or input differential pair (Q_1, Q_2) with one transistor feeding $2f_{LO}$ to each multiplier. The input pair isolates the divider's core from preceding stages. Sharing bias current reduces the number of devices in the $2f_{LO}$ path, thereby extending the operational bandwidth and reducing power consumption. Bias for the input pair is set by emitter resistor R_{EE}, resistors R_{iso} and R_b, and MOS devices M_1, M_2.

The output voltage swing of the divider in Fig. 8 is related to the product of the current I_{EE} (through R_{EE}) and load resistor R_C. The phase shift across each stage must be 90°, therefore the circuit is operating above its −3 dB bandwidth and the output amplitude is below its low frequency value ($I_{EE} \cdot R_C$). Load resistor R_C (typically on the order of kΩ) combined with parasitic capacitances at the upper differential amplifier outputs (i.e., collectors of pairs Q_3, Q_4 and Q_5, Q_6) dominate the overall response. The other poles in the circuit lie well above the lower cut-off frequency due to the emitter follower buffers placed between the two stages (Q_7, Q_8 and Q_9, Q_{10}). The followers add little phase shift to the signal but are able to drive the following input with a relatively low impedance, thereby reducing the effect of input parasitics on the upper differential pairs' frequency response. It should be noted that the input and output voltage swings of each stage are approximately equal due to amplitude limiting, so the Miller effect caused by collector-base feedback does not dominate the response as the voltage gain is almost unity. As a result, the output amplitude decreases at 6 dB per octave and the phase shift is a weak function of frequency close to 90°.

The design objectives for the divider stage are: total current consumption less than 2 mA, output voltage swing of

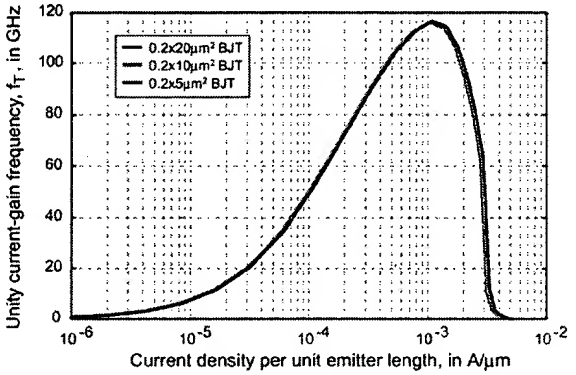

Fig. 9. f_T versus current density for IBM 7HP SiGe bipolar transistors.

100–200 mV_{peak} (differential), and an input frequency range from 9.6–12.4 GHz (or 4.8–6.2 GHz at the output). This covers the 5.3- and 5.8-GHz bands used for IEEE802.11a WLAN with a comfortable margin, and would drive an up- or downconverting Gilbert-type mixer in a transceiver.

The bias current for the upper differential pairs is set at 100 μA using resistor R_{EE}. This gives a transistor transit frequency (i.e., f_T) of approximately 12 GHz for the 5-μm-long devices selected for Q_3, Q_4 and Q_5, Q_6; this is well below the peak f_T of 110 GHz shown in Fig. 9, but reduces power consumption. Biasing the differential pairs via emitter followers ensures a working voltage of close to 1.8 V between collector and emitter (i.e., V_{CE}). Note that the lower pair Q_1, Q_2 operates at double this current density, therefore these 5-μm-long devices have more than double the f_T of the upper differential pairs. The minimum V_{CE} for these devices is 0.45 V assuming a 2.7-V supply. The followers are operated at approximately 40-GHz f_T (10 μm emitter length, 800 μA bias current). A larger transistor area is used for the followers to reduce the extrinsic base resistance, which causes ringing and instability in the response of bipolar transistors. Load resistor R_C is chosen to be 3.5 kΩ, which gives a differential output of 65 mV_{peak} at a free-running frequency of 9 GHz. The free-running frequency (i.e., with no ac applied at inputs to Q_1, Q_2) is set higher than the desired operating band to ensure proper operation despite processing variations.

B. Quadrature Phase Tuning

The phase angle between the I and Q outputs can be adjusted by deliberately introducing asymmetry into the circuit. Since the frequency of the oscillator is fixed by injection-locking to the $2f_{LO}$ input signal, the phase relationship between the outputs is changed. This is done in a controlled way by modifying the dc bias currents of the input emitter-coupled pair, or Q_1, Q_2 in Fig. 8. In this way, the phase delay through one stage increases, while the delay through the other stages is reduced.

CMOS FETs, M_1 and M_2 (see Fig. 8), are used as variable resistors for this purpose. This allows the offset in dc bias between Q_1 and Q_2 to vary over a wide range of differential tuning voltage (i.e., $V_{tune}^{+} - V_{tune}^{-}$). Resistors R_{iso}, isolate the $2f_{LO}$ input from the parasitics of transistors M_1 and M_2.

It should be noted that the amplitude of the divider output is also affected as the bias current is varied to adjust the I-Q phase. However, gain and amplitude limiting in the quad of a Gilbert mixer ensures that any differences in the LO amplitude which result from phase tuning are removed. Thus, when the bias currents are varied slightly in order to adjust the phase by a few degrees (as would be required for phase tuning), the effect at the output of an upconverting or downconverting mixer is negligible. This has been demonstrated in a 5-GHz image-reject receiver application [11]. In the circuit from [11], the I and Q outputs of the divider drive dual doubly balanced mixers in a Weaver downconverter. Over 40 dB of image rejection is realized with equal bias currents flowing in the two stages of the divider, and over 80 dB of image rejection through the use of phase tuning by manually adjusting the bias current in each stage of the divider. In this work, the MOSFET stage facilitates electronic control of the bias point and I-Q phase relationship, and similar results for image rejection in a transceiver application are expected.

C. Results

Simulations predict that a minimum input amplitude of 50 mV_{peak} (differential) is required to synchronize the divider at 5.5 GHz (i.e., 11-GHz input frequency). The output amplitude at 5.5 GHz is 120 mV_{peak} diff. An output frequency range from 4.4 to 13 GHz is realized for a 100-mV_{peak} input at $2f_{LO}$, whereas only 4.8–6.2 GHz is required. These input signal levels are compatible with the output available from the multiplier circuit, and even greater frequency range is achievable if a larger input amplitude is applied. The simulations also predict that output amplitude varies from approximately 200–100 mV_{peak} (differential) over the 5–6-GHz frequency range, which is more than needed to drive an active mixer.

A standalone test circuit for the divider was built and tested. In order to interface the divider outputs to 50-Ω measuring instruments, the open collector buffer stage of Fig. 3 is used. The divider test circuit is packaged in a 32-pin CQFP and consumes 9.5 mW from a 2.7-V supply. Measurements of the divider's input sensitivity (see Fig. 10) show that it divides properly with a (max.) −16 dBm amplitude (i.e., 50 mV_{peak}) input at frequencies above 6 GHz. Only −33 dBm (7.1 mV_{peak}) is required at the self-oscillation frequency (i.e., 16-GHz input/8-GHz output). This high sensitivity enables the divider to reliably detect the relatively small output voltage swing from

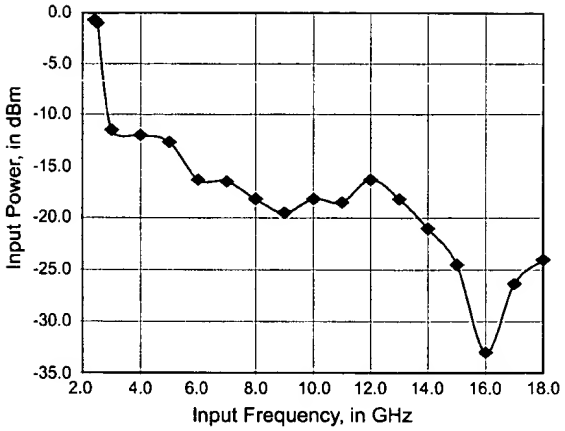

Fig. 10. Measured minimum input power versus locking range of the packaged divider test circuit.

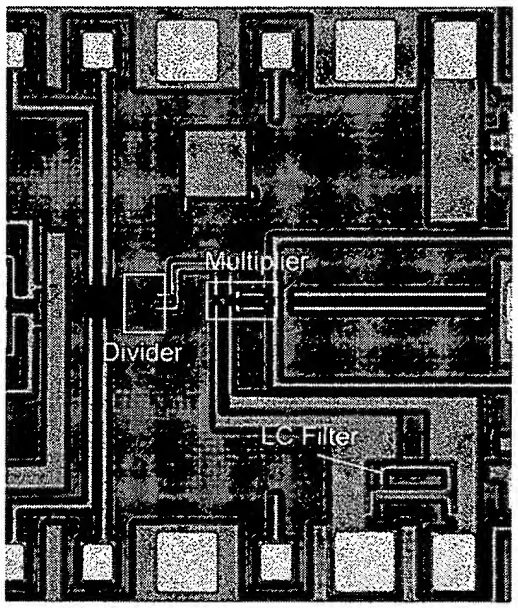

Fig. 11. Photomicrograph of the test chip.

the multiplier. A overall input frequency range of 2.4–18 GHz was measured for the standalone test circuit. However, the upper frequency limit was constrained by the test setup (input clock balun) and package parasitics (e.g., bondwire and package lead inductances), not the actual circuit.

V. Integrated I/Q Generator

The frequency multiplier and divider cascade were integrated together to investigate the overall phase noise behavior. This design was also fabricated in IBM's SiGe BiCMOS-7HP technology. The frequency multiplier and divider cascade, or quadrature phase generator, occupies an active chip area of 0.26×0.11 mm^2. A photomicrograph of the test chip showing the multiplier and divider blocks appears in Fig. 11. Care was taken in the physical layout to minimize high-frequency signal line lengths to reduce parasitics. Differential signal paths are used throughout to maximize sub-circuit isolation and minimize the effects of interconnect inductance. Additionally, all input

TABLE I
SUMMARY OF TEST RESULTS

Parameter	Specification	Measurement
Supply Voltage, in V	2.7	2.7
I/O Impedances, in Ω	50	50
Frequency Multiplier		
Input Frequency Range, in GHz	4.5-6.5	4.0-7.0
Input Power, in dBm	0	4
Attenuation, in dB	15-20	25.3
Power Consumption, mW	10	12.5
Frequency Divider		
Input Frequency Range, in GHz	8-14	4.8-18
Min. Input, in dBm	-15	-16
Power Consumption, mW	10	9.5
I/Q Generator		
Power Consumption, in mW	20	23
Active Chip Area, in mm^2	-	0.26x0.11
Bandwidth, in GHz	4.5-6.5	1.2-9.0
Residual Phase Noise, in dB	-	±0.45 (max)
I/Q Phase Tuning Range, in degrees	±22	±15
I/Q Phase Tuning Accuracy, in deg/mV	0.04deg/mV	0.033deg/mV

and output signal paths connected to I/O pads are designed to have 50-Ω characteristic impedance. Substrate coupling between different circuit blocks was minimized by grounded p+ diffusions. Substrate coupling between the multiplier's core circuit and its surrounding biasing and buffering circuits is minimized by use of separate supply lines decoupled with the on-chip *LC* notch filter.

The test chip is packaged in a standard 32-pin CQFP and mounted into a custom test fixture for evaluation. Bondwire self-inductance is estimated at 1.2–1.5 nH. The package lead inductance depends upon position, with leads close to the corners of the package having a larger inductance than midway along each side. RF signals were restricted to the low inductance leads, which are on the order of 2 nH each. The overall inductance of a differential interconnection is less than the self-inductance of a given lead/bondwire combination because of mutual magnetic coupling between adjacent conductors. Even so, the total interconnect inductance is estimated at 2.3 nH, and the 5–6-GHz signal from the test chip is attenuated by 80 Ω of inductive reactance in series with each output. Moreover, shunt capacitive parasitics from I/O pads, the package and the PCB combined with the parasitic inductances form a low-pass filter that attenuates signals above 6 GHz. As the test equipment is single-ended, only one output is used while the other is terminated with a 50-Ω load. This 3-dB loss has been taken into account in Table I, which summarizes the measured and simulated results for all three circuits tested (i.e., multiplier, divider, and the complete quadrature phase generator). Note that the bandwidth achieved by the I/Q demonstrator is much greater than required for the 5–6-GHz WLAN application, a very small chip area is needed to integrate the active circuits, and electronic phase tuning range of the outputs of almost 30° (wider than needed for trimming) is possible.

The measured phase noise of the quadrature generator for a 5.5-GHz input as well as the phase noise of the 5.5-GHz source alone are shown in Fig. 12. We estimate the error in the phase noise measurement at ±0.5 dB. The externally variable phase-tuning voltages (V_{tune}^{+} and V_{tune}^{-} of Fig. 8) were grounded for this measurement. Note that the residual phase noise (i.e., difference between source and quadrature generator output) between 100-Hz and 100-kHz offset from the LO input frequency is typically less than 0.5 dB which is within the error of the phase noise measurement system. Measurements up to 3-MHz offset were made, and the output noise was observed to track the input phase noise at these higher offsets frequencies. Functionality of the phase tuning inputs was confirmed using a high-speed oscilloscope, however, this measurement is only accurate to within about 5°. A phase tuning range on the order of ±15° for a 1-V change in the differential phase tuning voltage ($V_{\text{tune}}^{+} - V_{\text{tune}}^{-}$) was measured.

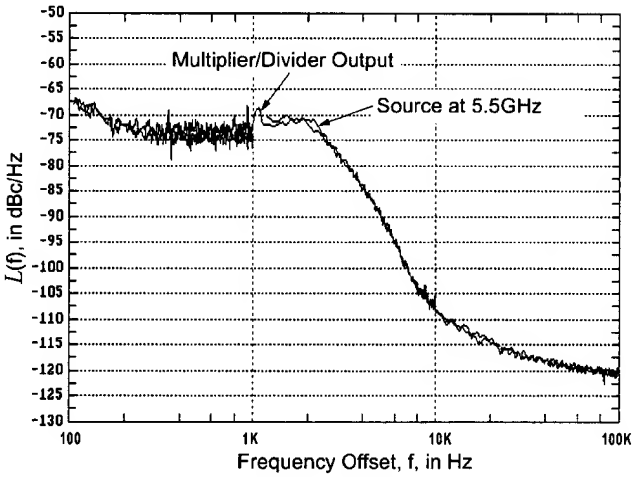

Fig. 12. Measured phase noise of multiplier/divider cascade for a 5.5-GHz input.

VI. Summary

The cascade of a new wide-band frequency multiplier and a regenerative divide-by-2 with quadrature outputs exploits the high input sensitivity and low power properties of the analog divider. The cascade allows precise phase adjustment for maximum sideband suppression in a 5–6-GHz radio transceiver application and results in minimal residual phase noise at the output. The LO source chain presented here offers the flexibility needed to optimize power consumption and phase noise (i.e., optimize VCO, multiplier, and divider independently), which may result in lower overall power consumption.

In operation, the quadrature phase generator consumes 23 mW from a 2.7-V supply. Power consumption could be reduced by lowering the supply voltage to 1 V for the multiplier and 2.2 V for the divider [11]. However, it is also possible to trade off operating bandwidth for lower current consumption in both multiplier and divider circuits. For example, the frequency multiplier has an upper −3 dB frequency of about 78 GHz (simulated). The load resistance could therefore be increased to maintain output voltage swing at the expense of bandwidth, but at a lower current draw. Simulations show that current consumption could be reduced by a factor of 3 while maintaining an output swing of 100 mV_{peak} at 12-GHz output (6-GHz input) and over 25-GHz maximum output bandwidth. Similarly, the operating margin in the divider could be reduced by using less current to bias the emitter followers. Reducing the bias current from 800 to 200 μA saves a total of 2.4 mA, while reducing the max input frequency to 18 GHz. This is still more than adequate for the divider and comparable to the supply current that would be required by an output buffer for an I/Q VCO. Thus, from this study it is expected that a quadrature generator consuming less than 8 mW at 2.7 V could be built that still maintains adequate frequency margin for the 5–6-GHz WLAN application.

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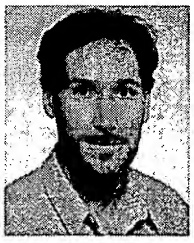

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